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PATENT
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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 19 – 23 remain.

Claims 19, 22, and 23 are being amended.

Claims 1 – 18 and 24 – 40 have been cancelled.

WHAT IS CLAIMED IS:

1. – 18. (Cancelled)

19. (Currently Amended) An attenuator comprising:

a first stage comprising:

a first operational amplifier;

a tapped resistor having an input for receiving input data, an output coupled to an output of said first operational amplifier, and a plurality of taps for selectively presenting a sequence of voltages to a [[said]] noninverting input of said first operational amplifier, each of said sequence of voltages corresponding to an attenuation step, said first stage in response to said sequence of voltages stepping an attenuation produced by said attenuator from an intermediate value to a predetermined ending value; and

a second stage comprising:

a second operational amplifier;

a tapped resistor having an input for receiving analog data from said first

stage, an output coupled to an output of said second operational amplifier, and a plurality of taps for selectively presenting a sequence of voltages to a noninverting input of said second operational amplifier, each of said sequence of voltages corresponding to an attenuation step, said second stage stepping said attenuation for a predetermined starting value to said intermediate value.

20. (Currently Amended) The attenuator of Claim 19 wherein [[said attenuator of]] said first stage responds to a first set of control bits and [[said attenuator of]] said second stage responds to a second set of control bits received by said attenuator.

21. (Original) The attenuator of Claim 20 wherein an attenuation of said second stage is fixed at said intermediate value when a one of said first set of control bits is received by said attenuator.

22. (Currently Amended) The attenuator of Claim 19 wherein each said tapped resistor comprises:

a plurality of resistors coupled in series, a [[said]] tap disposed between selected pairs of said resistors, values of said resistors predetermined to provide a predetermined voltage at each [[said]] tap; and

a decoder for selectively coupling a said tap to said non – inverting input of [[a]] said amplifier of a corresponding stage.

23. (Currently Amended) The attenuator of Claim 20 wherein said decoder comprises a plurality of decoding circuits each for controlling a corresponding one of said taps, each said decoding circuit comprising:

output drive circuitry;

a plurality of transistors coupled in series for selectively activating and deactivating a corresponding decoder output line through [[said]] output drive circuitry; and

a plurality of inverters selectively coupled to gates of said transistors such that

said transistors activate and deactivate said corresponding output upon receiving an assigned subset of a selected one of [[said]] first and second sets of bits.

24. – 40. (Cancelled)